REMARKS

Claims 1-8 are pending in the application. Applicants amend claims 1-4, 6, and 8 for further clarification No new matter has been added.

Applicants, again, acknowledge with appreciation the Examiner's allowance of claims 5 and 7.

Claims 1-4, 6, and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Japanese Patent Application Publication No. 05-292050 to Kazawa et al. in view of U.S. Patent No. 5,680,246 to Takahashi et al. Applicants amend the rejected claims in a good faith effort to further clarify the invention as distinguished from the cited references, and respectfully traverse the rejection.

Kazawa et al. describe a high speed overhead processing section 3 for multiplexing signals that a low speed overhead processing section 2 has processed. The high speed overhead processing section 3 only multiplexes signals by byte-interleave, and does not multiplex signals by bit-interleave because Figs. 1, 2, and 5 of Kazawa et al. clearly show that A1, A2, and C1 bytes are not multiplexed by bit-interleave, but are multiplexed by byte-interleave.

Kazawa et al. also describe inverting frame synchronization pattern A1 and A2 bytes for every byte and inserting "1010..." pattern to a high speed frame header. The inverting of frame synchronization pattern A1 and A2 bytes and the "1010..." pattern insertion are, again, by byte—consistent with the high speed overhead processing section 3 that multiplexes signals by byte-interleave and not bit-interleave.

Takahashi et al. describe,

> "[t]he present embodiment of the invention described subsequently relates generally to an optical transmission apparatus and more particularly to an optical transmission apparatus which outputs, upon restoration to an ordinary mark rate of about ½ after an input signal exhibits a succession of '1'

> (mark rate 1) or a succession of '0' (mark rate 0), signal light after a delay by a time longer than a gain response time of an optical amplifier." Col. 19, lines 19-26 of Takahashi et al.

And Takahashi et al., as cited and relied upon by the Examiner, fail to disclose or suggest multiplexing signals accommodated by low speed frames to a high speed frame by bit-interleave.

In other words, even assuming, arguendo, that it would have been obvious to one skilled in the art at the time the claimed invention was made to combine Kazawa et al. and Takahashi et al., such a combination would still have failed to disclose or suggest,

> "[a] time-division bit-interleave multiplexing method comprising:
> (a) a step of generating a plurality of first signals and a plurality of second signals to set in a second area of a low speed frame different from a first area of said low speed frame used for frame synchronization, and said second area of said low speed frame not used for frame synchronization ;
> (b) a step of generating low speed frames accommodating low speed signals of plural channels including said first and second signals and transmission signals;
> (c) a step of converting said first and second signals in said second area of each channel into either of "1/0" alternating signals, said "1/0" alternating signals being repeated patterns of bits "10", and "0/1" alternating signals, said "0/1" alternating signals being repeated patterns of bits "01"; and
> (d) a step of time-division ***bit-interleave*** multiplexing said low speed frames accommodating said low speed signals after said step (c), thereby producing a high speed frame accommodating high speed signals;
> wherein a main reiteration pattern of a pattern concatenated by a first reiteration pattern of a bit '1' or a bit '0,' a reiteration number of times of the first reiteration pattern being a number of the plurality of channels, and a second reiteration pattern of a bit '0' or a bit '1,' the reiteration number of times of the second reiteration pattern being the number of the plurality of channels, is mapped to a third area of said high speed frame by bit-interleave, and a mark rate in said third area becomes 50%," as recited in claim 1. (Emphasis added)

Accordingly, Applicants respectfully submit that claim 1 is patentable over Kazawa et al. and Takahashi et al., separately and in combination, for at least the foregoing reasons.

Claims 2-4, 6, and 8 incorporate features that correspond to those of claim 1 cited above, and are, therefore, patentable over the cited references for at least the same reasons.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

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